MULTIMEDIA UNIVERSITY

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FINAL EXAMINATION

TRIMESTER 1, 2019/2020

EEE 3156 DIGITAL SYSTEM
(EE Group)

21 OCTOBER 2019

9:00 AM – 11:00 AM
(2 Hours)

INSTRUCTION TO STUDENT

1.This Question paper consists of 4 pages including cover page with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1:

(a)   Create a truth table with input signals, S_2, S_1, S_0, A, B and output signal F, of the single bit Logic Circuit shown in Table Q1.

[8 marks]

Table Q1

$S_2S_1S_0$	Logic Operation
000	$F = \bar{A}$
001	$F = AB$
010	$F = A + B$
011	$F = A \oplus B$
100	$F = \bar{B}$
101	$F = \overline{AB}$
110	$F = \overline{A + B}$
111	$F = \overline{A \oplus B}$

(b)   Based on part (a), design a single bit Logic Circuit using some standard logic gates and a 8-to-1 multiplexer.

[10 marks]

(c)   Based on part (a), design a single bit Logic Circuit using the 4-input look up table (LUT).

[7 marks]

Question 2:

Refer to the binary coded decimal (BCD) to 7-segment decoder shown in Figure Q2.1.

(a)   Construct the truth table of the binary coded decimal to 7-segment decoder to display the following characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, b, C, d, E and F through the 7-segment display shown in Figure Q2.2. Given that the active high 7-segment display is used with LED on = '1' and LED off = '0'.
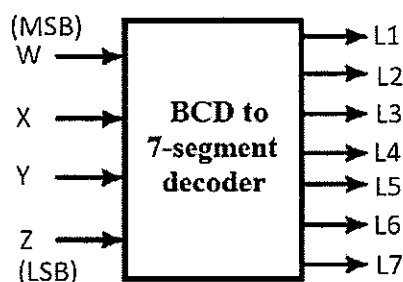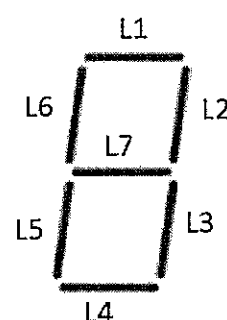
[16 marks]

Figure Q2.1

Figure Q2.2

(b)   Design the binary coded decimal (BCD) to 7-segment display decoder shown in Figure Q2.1 using programmable logic array (PLA).

[9 marks]

Continued ...

Question 3:

(a) Create the state assigned table of the 010 sequence recognizer shown in Figure Q3. Given that W = input signal and Z = output signal.
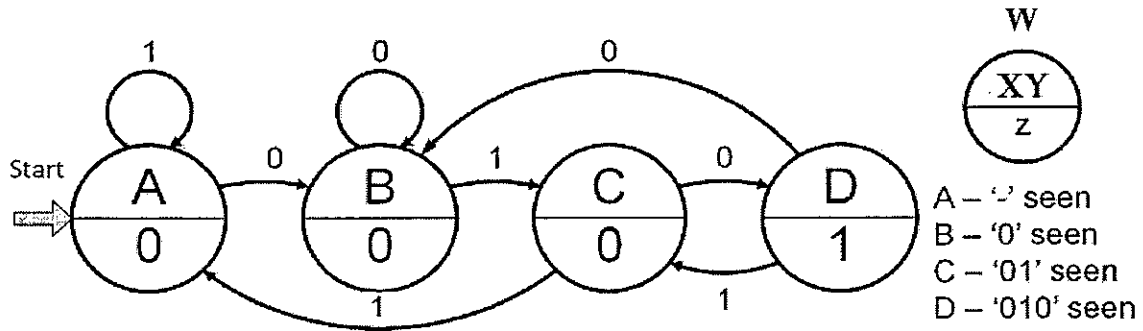
[5 marks]

Figure Q3

W

XY
Z

A – '-' seen
B – '0' seen
C – '01' seen
D – '010' seen

(b) Compute the simplified characteristic equations for the next state signals (X & Y) and output signal (Z) of the 010 sequence recognizer shown in Figure Q3.

[8 marks]

(c) Design the 010 sequence recognizer shown in Figure Q3 using standard logic gates and D flip-flops.

[7 marks]

(d) Design and sketch the state diagram of the 101 sequence recognizer.

[5 marks]

Question 4:

Refer to the Arithmetic and Logic Unit shown in Figure Q4.

Figure Q4
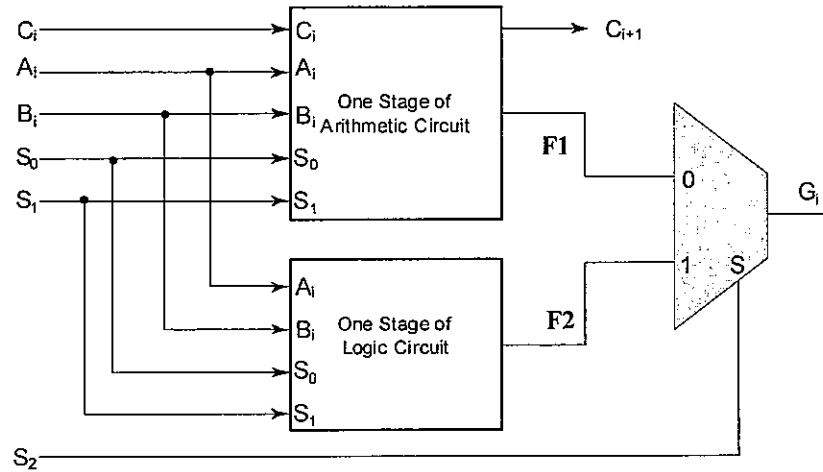
Table Q4.1

S_1S_0	Arithmetic Operations
00	F1 = A plus B
01	F1 = A plus B plus C_i
10	F1 = A plus $\bar{B}$
11	F1 = A plus $\bar{B}$ plus 1

Table Q4.2

S_1S_0	Logic Functions
00	F2 = A
01	F2 = $\bar{A}$
10	F2 = AB
11	F2 = A + B

(a)   Design a single bit full adder, with inputs C_{in}, A, B and outputs C_o, S.

[15 marks]

(b)   Design a One Stage of Arithmetic Circuit shown in Figure Q4 and the truth table shown in Table Q4.1 using a single bit full adder, multiplexers and standard logic gates.

[5 marks]

(c)   Design a One Stage of Logic Circuit shown in Figure Q4 with the truth table shown in Table Q4.2 using standard logic gates and multiplexer.

[5 marks]

End of Paper